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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,588	10/01/2003	Peter Beer	W&B-INF-1973	7991

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EXAMINER	
IQBAL, NADEEM	
ART UNIT	**PAPER NUMBER**
2114	

DATE MAILED: 05/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/676,588	BEER ET AL.	
	Examiner	Art Unit	
	Nadeem Iqbal	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *April 13, 04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Joo (U.S. Patent number 6198667).

3. As per claim 1, Joo teaches (col. 3, lines 40-42) a semiconductor memory device having a multi-bank memory array that accesses a plurality of banks when testing the multi-bank memory array. He also teaches (col. 3, lines 54-57) a bank selector for simultaneously row-accessing the plurality of memory banks, an input/output controller for outputting a plurality of write enable signals and a plurality of read enable signals. He thus teaches limitations pertain to a test system for testing a first memory circuit and a second memory circuit in parallel, a tester unit configured to generate a circuit select signal for activating the first and second memory circuits to receive signals. He also teaches (col. 3, lines 57-59) a buffer unit for transmitting externally applied data to the plurality of memory banks by being enabled by the plurality of write enable signals and coinciding and outputting data. He thus teaches limitations the first memory circuit and the second memory circuit each having a test data generator circuit for generating test data for writing to memory cells. As per limitations applying simultaneously the circuit select signal to the first memory circuit in inverted form and to the second memory circuit in noninverted form. He teaches (col. 3, lines 53-55).

4. As per claim 2, With reference to an inverter unit connected between the first memory circuit and the tester unit. He teaches (col. 3, lines 54-56).

5. As per claim 3, With reference to configured to test a plurality of first memory circuits and/or a plurality of second memory circuit. He teaches (col. 4, lines 1-4).

6. As per claim 4, With reference to at least one of the first and second memory circuits is a DRAM memory circuit. He teaches (col. 3, lines 44-46).

7. As per claim 5, Joo substantially teaches the claimed invention as disclosed related to claim 1 above. He also teaches (col. 3, lines 54-57) a bank selector for simultaneously row-accessing the plurality of memory banks, an input/output controller for outputting a plurality of write enable signals and a plurality of read enable signals. He thus teaches limitations pertain to a memory circuits configured to be activated in dependence on a circuit select signal. He also teaches (col. 3, lines 57-59) a buffer unit for transmitting externally applied data to the plurality of memory banks by being enabled by the plurality of write enable signals and coinciding and outputting data. He thus teaches limitations enabling the first and second memory circuits to receive a control signal, the control signal initiating a function in the respective memory circuit depending on an activation of the first or second memory circuit. As per limitations applying simultaneously the circuit select signal the first memory circuit in inverted form and to the second memory circuit in noninverted form. He teaches (col. 3, lines 53-55).

8. As per claim 6 With reference to applying the control signal to a signal input of the respective memory circuit. He teaches (col. 3, lines 54-56).

9. As per claim 7, With reference to setting the circuit select signal to a first state for activating the first memory circuit and deactivating the second memory circuit, and setting the

circuit select signal to a second state for activating the second memory circuit and deactivating the first memory circuit in the second state. He teaches (col. 4, lines 1-4).

10. As per claim 8, With reference to the control signal is at least one signal selected from the group consisting of a RAS signal, a CAS signal, and a WE signal. He teaches (col. 3, lines 54-57, Fig. 5).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nadeem Iqbal whose telephone number is (571)-272-3659. The examiner can normally be reached on M-F (8:00-5:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571)-272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nadeem Iqbal
Primary Examiner
Art Unit 2114

NI